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Design and Implementation of Low Power and High Speed Shift Register Using Fin FET

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Abstract: *The electrostatic benefit of using a silicon-on-insulator wafer substrate versus a bulk-silicon wafer substrate with optimized supersteep retrograde doping for a low-power 7-/8-nm.SOI FinFET technology is projected to provide only slight improvement in performance and minimum cell operating voltage as compared with SSR FinFET technology. In this work we are applying valuable power gating schemes to FinFET based shift register to enhance its performance by reducing the leakage current in standby mode. This provides the motivation to explore the design of low leakage FinFET based Shift register with power reduction techniques.*
Keywords: *SOI FinFET, Low Power, D Flip-Flop, SVL Techniques, Types of Shift Register.*

I. Introduction

BULK-SILICON (Si) trigate transistors have been adopted by the industry since the22-nm CMOS technology node to facilitate further component miniaturation. The use of a silicon-on-insulator (SOI) substrate eliminates sub-fin leakage current in FinFETs without the need for "punch through stopper" (PTS) doping at the base of the gated fin region, and hence provides for improved transistor performance as well as reduced variation arising from random dopant fluctuations (RDFs). Even for the idle circuit Metal Oxide Semiconductor (MOS) devices will not able to properly turn-off, as a result of which "off-state current" will flow through the circuit. The major sources for this off-state current: (1) Sub-threshold leakage, (2) Gate leakage current and (3) Band-to- Band tunneling leakage current. In this paper, we propose three circuit techniques to control the off-state current, using different PULL-UP and PULLDOWN networks of NMOS and PMOS are applied to FinFET based Shift register one after another. Due to this treatment of PULL-UP and PULLDOWN network controlled voltage supply is obtained and the current driving capability of the design is increased, hence less Gate leakage current is formed.

II. Device Simulation And Design Optimization

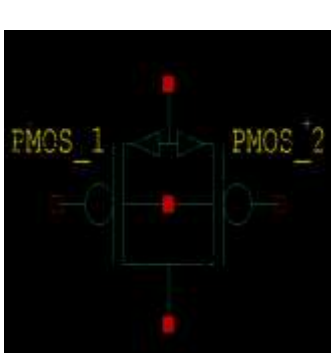


Fig.1.1 Shematic of FinFET **Fig.1.2** schematic of SVL technique

A.FINFET

FinFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed. The main characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name. The thickness of the fin determines the effective channel length of the device. In terms of its structure, it typically has a vertical fin on a substrate which runs between a larger drain and source area. This protrudes vertically above the substrate as a fin. The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel. This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects.

B. SVL TECHNIQUES

Leakage current flowing through OFF transistors is reduced in above circuit by applying SVL technique as shown in Fig. Leakage current flowing through OFF transistors is reduced in above circuit by applying SVL technique as shown in Fig. 4 This technique is implemented in the upper side as PULL UP network connected to the supply Vdd and lower side as PULL DOWN network connected with ground of 5T DFF .The PULL UP network contain one PMOS (Psw1) switch which is connected in parallel with a NMOS (Nsw1) switch such that during active mode as Clk is high which causes Psw1 switch to turn ON hence connecting the basic 5T D flip flop to Vdd supply voltage while during the standby mode of operation Clk is low turning ON the Nsw1 switch which provides virtual supply to 5T DFF. In the lower side SVL one PMOS switch is again in parallel connection with one NMOS switch so in active mode NMOS switch (Nsw2) turns ON connecting ground to 5T DFF while in standby mode PMOS switch Psw2 turn ON and provide virtual ground to the basis 5T DFF. The switch Psw1 and Nsw2 together in active mode connects the Vdd and the ground to 5T DFF for normal circuit operation but during the standby mode for controlling the leakage current through OFF transistors the Nsw1 and Psw2 switches provides virtual supply and virtual ground which reduces the sub leakage current in OFF transistors.

B.1.UPPER SVL TECHNIQUE:

In U-SVL technique, a combination of one PMOS & two NMOS are connected in parallel. So that an input clock pulse is applied at the PMOS of circuit of U-SVL and rest of all NMOS are connected to drain terminal. Shift register using U-SVL scheme is depicted in Figure below. Under this scheme, full supply voltage of Vddisapplied to the semiconductor device. The U-SVL schematic is intended on a broad channel pull up pMOSFET& pull down n-MOSFET. The circuit diagram of shift register designed using U-SVL technique. This approach is more valuable for reducing the power consumption also for the leakage current. For very low Power consumption, U-SVL technique is most responsible. Shift register designed at micron CMOS technology, produces the better results. But now a day of nanotechnology at Vdd = 0.7 V, power consumption.

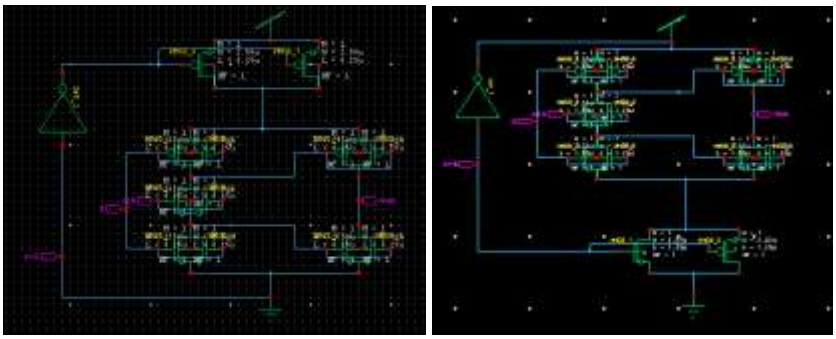


Fig 1.3 Upper SVL techniqueFig.1.4Lower SVL technique

B.2. LOWER SVL TECHNIQUE

In L-SVL technique a combination of one NMOS & two PMOS are connected in parallel. So that an input clock pulse is applied at the NMOS of circuit of L-SVL and rest of all PMOS are connected to ground. This ground terminal is connected to the LSVL circuit. Shift register using L-SVL scheme is shown in Figure 3. The switch brings 0Volt at the ground node & raises the ground level (virtual ground). The L-SVL circuits initiates wide channels pull down n-MOSFET and pull up p-MOSFET.Depending upon the clock and inputs, variation in output is varied. Figure 3 shows the variation of power Vs supply voltage of shift register design using L-SVL scheme. Where the power consumption is measured at the various supply voltage at Vdd = 0.7 V, power consumption is 1.24μw.

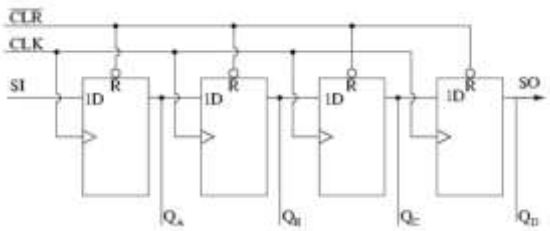
C. SHIFT REGISTER

A shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the 'data' input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the 'bit array' stored in it, 'shifting in' the data present at its input and 'shifting out' the last bit in the array, at each transition of the clock input. More generally, a shift register may be multidimensional, such that its 'data in' and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and

parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L.

TYPES OF SHIFT REGISTER



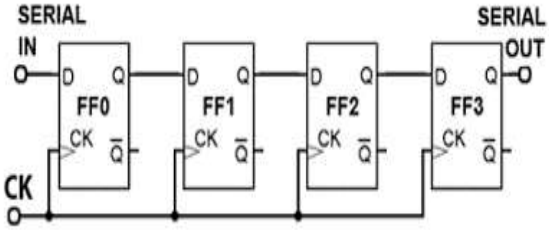
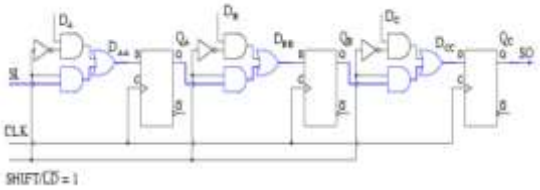


Fig 1.5 Serial-in to Parallel-out (SIPO) **Fig 1.6** Serial-in to Serial-out (SISO)



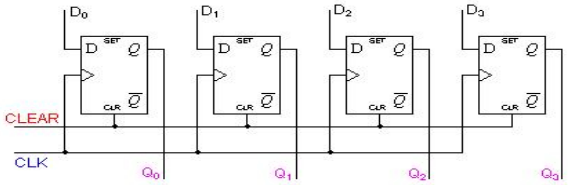


Fig.1.7 Parallel-in to Serial-out (PISO) **Fig.1.8.**Parallel-in to Parallel-out (PIPO)

- **Serial-in to Parallel-out (SIPO) -**The register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel.
- **Serial-in to Serial-out (SISO)** - The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- **Parallel-in to Serial-out (PISO)** - The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- **Parallel-in to Parallel-out (PIPO)** - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

D. SIMULATED OUTPUT

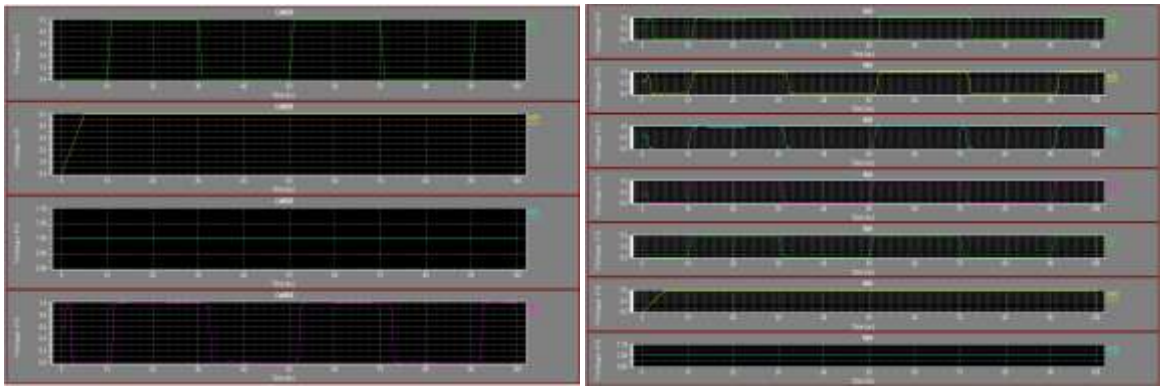
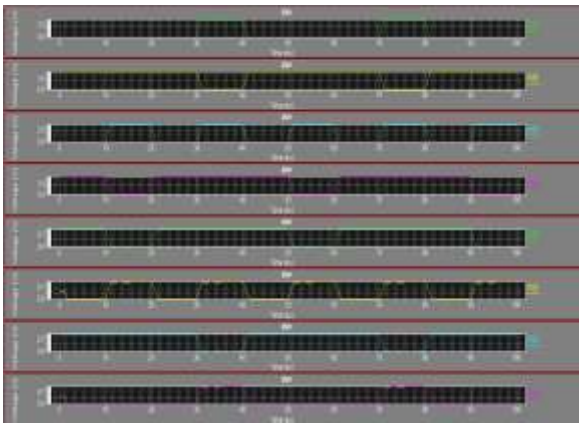


Fig 1.9 Serial in serial out(SISO) **Fig 1.10** Serial in parallel out(SIPO)



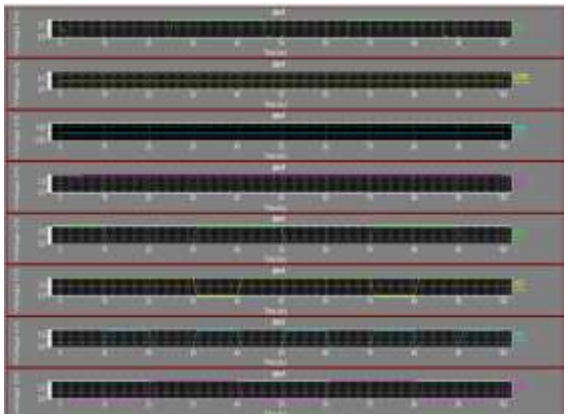


Fig 1.11 Parallel in parallel out(PIPO) **Fig 1.12** Parallel in serial out(PISO)

III. Results

Table.1.1 Comparison of CMOS shiftTable 1.2 Comparison of shift register register and FinFET shift registerwith and without SVL

Parameters	**CMOS shift register**	**FinFET shift Register**
Power consumption	4.954777e-007 watts	1.090036e-006 watts
Delay measurement	-3.4599e-008	-3.8195e-008

Parameter	**Shift register with SVL technique**	**Shift register without SVL technique**
Power consumption	1.007419e-006 watts	1.090036e-006 watts
Delay measurement	-3.8195e-008	-3.8579e-008

Table.1.4 Comparison of types of shift register using FinFET and SVL technique.

PARAMETER	**SISO**	**SIPO**	**PIPO**	**PISO**
Power	1.007419e-006 watts	1.039051e-006 watts	1.183502e-006 watts	1.666446e-006 watts

IV. Conclusion

CMOS and SOI FinFET with SVL technologies are projected to provide substantial reductions in power and increase in speed for minimum 5T-shift register. The proposed circuit is a low power consumption design forSVL based shift register with power reduction of 83mW. The delay is reduced by FinFet technology by 38ns. The design overcomes short channel effects as the calculated leakage current is very small in comparison with the leakage which occur in conventional SR based DFF. Thus total power dissipated in the proposed circuit gets reduced.

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